Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the subject application, and please amend the claims as follows:

1. (Currently amended): A mounted semiconductor assembly comprising:

a semiconductor assembly consisting of a single semiconductor die ~~or a plurality of semiconductor dies consisting of a first chip and one or more second chips stacked or flip-mounted thereon~~;

a first portion consisting of a base support with heat conducting surface for mounting the semiconductor assembly and peripheral electrical connectors;

a second portion having a heat radiating surface ~~portion~~; and

a connecting portion joining the first and second portions and arranged to allow folding of the second portion over the first portion to form a cover, wherein the mounting comprises a sealing material completely encapsulating the connecting portion at least partially encapsulating the mounting and the semiconductor assembly such that at least part of a printed circuit board facing surface of the first portion base support and peripheral electrical connectors and[[/or]] the heat radiating surface of the second portion are left exposed and fixed in a position planar to the sealing material defined component outline and where the first and second portions have features for the provision of additional locking strength between the mounting and the sealing material.

2. (Canceled)

3. (Currently amended): A mounted semiconductor assembly according to claim 1 wherein the first portion of the mounting comprises a formation of a base support and electrical connectors each of which has a printed circuit board facing ~~said~~ surface, which is not covered by said sealing material.

4. (Previously presented): A mounted semiconductor assembly according to claim 1, wherein the second portion is arranged to be in a spaced parallel relationship with the first portion.

5. (Previously presented): A mounted semiconductor assembly according to claim 1, wherein the second portion further comprises at least one additional edge portion arranged to extend when the mounting is folded beyond at least one edge of the first portion of the mounting.

6. (Withdrawn): A mounted semiconductor assembly according to claim 5 wherein the mounting is in the form of an EMI enhanced package wherein the second portion is provided with four additional edge portions to define four walls to protect the semiconductor assembly.

7. (Previously presented): A mounted semiconductor assembly according to claim 1, wherein the mounting is formed from a single sheet of electrically and thermally conducting material.

8. (Previously presented): A mounted semiconductor assembly according to claim 1, wherein the connecting portion is provided with folding means to enable the folding of the second portion over the first portion.

9. (Withdrawn): A mounted semiconductor assembly according to claim 1, wherein the mounting is provided with a third portion and second folding portion arranged to allow folding of the third portion over the second portion to form said cover, such that the third portion is in a spaced parallel relationship with the first portion and second portion.

10. (Withdrawn): A mounted semiconductor assembly according to claim 1, wherein the mounting further comprises a means for mounting surface mount technology (SMT) component which is a passive component.

11. (Withdrawn): A mounted semiconductor assembly according to claim 10 wherein the SMT mounting means comprises one or more recesses in the second portion.

12. (Withdrawn): A mounted semiconductor assembly according to claim 1, wherein the cover is patterned or formed to function as a passive component which is an antenna, an inductor, an interdigitated capacitor, a parallel plate capacitor, a microstrip coupler, a filter or combinations thereof.

13. (Withdrawn): A mounted semiconductor assembly according to claim 1, wherein the mounting further comprises means adapted for mounting a sensor semiconductor assembly, the sensor mounting means is adapted for mounting an image sensor semiconductor assembly, biometric sensor semiconductor assembly, pressure sensor semiconductor assembly or combinations thereof.

14. (Withdrawn): A mounted semiconductor assembly according to claim 1, wherein the cover is adapted to provide direct access to the semiconductor assembly, such direct access means comprises an aperture in the cover.

15. (Withdrawn): A mounted semiconductor assembly according to claim 14 wherein the mounted semiconductor assembly is further adapted to mount an optical component in relationship to an image sensor semiconductor chip.

16. (Withdrawn): A mounted semiconductor assembly according to claim 14 wherein the direct access means is further defined by having one or more recesses about its perimeter, which recesses face towards, or away from, a mounted semiconductor assembly.

17. (Withdrawn): A mounted semiconductor assembly according to claim 16, wherein the direct access means or the recesses can be used to locate a further component for use in the semiconductor assembly.

18. (Withdrawn): A mounted semiconductor assembly according to claim 1, wherein the mounting further comprises one or more recesses formed within the cover into which mould material can flow to secure the cover.

19. (Withdrawn): A mounted semiconductor assembly according to claim 1, which further comprises a means to permit coupling of selected frequencies of electromagnetic radiation through the mounting, the frequency coupling means comprises one or more apertures in the cover of appropriate dimension to permit coupling at a selected frequency.

20. (Previously presented): A mounted semiconductor assembly according to claim 3, wherein the formation of electrical connectors is in a spaced relationship with the first portion and are linked electrically with the semiconductor assembly.

21.-22. (Canceled)

23. (Withdrawn): A mounted semiconductor assembly according to claim 1, wherein the mounting further comprises a heat dissipation means to provide a low thermally resistive path between a mounted semiconductor assembly and the cover of the package.

24. (Previously presented): A mounted semiconductor assembly according to claim 1, wherein the mounting is part of an array of a plurality of mountings.

25.-40. (Canceled)

41. (Canceled)

42. (Canceled)

43. (Previously presented): A mounted semiconductor assembly according to claim 7 wherein the single sheet of electrically and thermally conducting material is copper.

44. (Previously presented): A mounted semiconductor assembly according to claim 8 wherein the folding means is at least one weakened line in the mounting having a thickness that is less than that of the rest of the mounting.

45. (Previously presented): A mounted semiconductor assembly according to claim 44 wherein the at least one weakened line is a scored line or an etched line in the mounting.

46. (Previously presented): A mounted semiconductor assembly according to claim 8 wherein the folding means includes two weakened lines, one between the first portion and the connecting portion and one between the second portion and the connecting portion.

47. (Previously presented): A mounted semiconductor assembly according to claim 1 wherein the second portion is continuous.

48. (Previously presented): A mounted semiconductor assembly according to claim 1 wherein the second portion functions as a heatsink.

49. (Previously presented): A mounted semiconductor assembly according to claim 1 wherein the second portion functions as a low resistance and low inductive path to ground.

50. (Previously presented): A mounted semiconductor assembly according to claim 1 wherein the second portion functions as a local electromagnetic shield.